REMARKS

The Examiner raised §112 concerns about claims 3, 4, 6, 8 and 21-23. In response, we have amended claim 1 by reciting the inverse-free Berlekamp-Massey algorithm and we have defined the mathematical symbol "t" as an integer indicating the degree of the polynomial for which coefficients are determined. We have also amended claim 1 to recite (t+1) finite field multipliers. Finally, we have added a new claim 24 which recites that the system includes (2t+1) finite field adders.

The Examiner rejected claims 1, 2, 4, 5, 7, 9, 10, 14, 15, and 21 under 35 U.S.C. §102(a) as anticipated by U.S. 6,493,845 to Shen. We note however, that claim 1 now explicitly relates to a data processing system for the Berlekamp-Massey algorithm that includes (t+1) finite field multipliers. In contrast, Shen describes Fettweis-Hassner systems for producing R error correction code (ECC) redundancy symbols or R error syndromes (see col. 4, lines 7-8 and col. 6, lines 17-20). There are R multipliers in the system shown in Fig. 1 of Shen (see col. 1, lines 17-18). R in Shen may be similar to 2t in the present application, as there are 2t syndromes S_1 in the syndrome polynomial S(x) in the present application, although it is noted that the systems in the present application and Shen implement different algorithms. Therefore, there are 2t multipliers in the system of Fig. 1 of Shen, and even more in systems shown in Figs. 3 and 4 (e.g. se col. 7, line 67 to col. 8, line 3). Therefore, Shen shows a system that does not implement the Berlekamp-Massey algorithm, and has more than (t+1) finite field multipliers.

The Examiner rejected claims 1-17 and 21-23 under 35 U.S.C. 102(a) as anticipated by U.S. 7,051,267 to Yu et al.

We note, however, that Yu shows in Fig. 6A a system for implementing the Berlekamp-Massey algorithm where t=3 (see col. 2, line 44 and col. 3, line 59). The system of Fig. 6A includes (3t+3) multipliers. Another embodiment, shown in Fig. 2, includes (2t+2) multipliers. Thus, both of these systems include more than (t+1) multipliers, contrary to the requirements of claims 1 as now amended.

In other words, both Shen and Yu describe systems that have at least double the number of multipliers as that required by the claimed invention. Having fewer multipliers has clear benefits in terms of circuit complexity, chip area, power consumption and/or circuit speed.

For the reasons stated above, we believe that the claims are in condition for allowance and therefore ask the Examiner to allow them to issue.

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Respectfully submitted,

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